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PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10082055	FILING DATE 02/26/2002	CLASS 302	SUBCLASS 117	GAU 2173	EXAMINER <i>Ravenard</i>
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2857

\*\*CONTINUING DATA VERIFIED:

\*\* FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-269216 09/05/2001

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed		<input type="checkbox"/> yes <input type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met		<input type="checkbox"/> yes <input type="checkbox"/> no	100021-00072
Verified and Acknowledged Examiners's initials			
TITLE : Test circuit and semiconductor integrated circuit effectively carrying out verification of connection of nodes			
U.S.DEP'T. OF COMM./PAT. & TM-PTO-436L(Rev. 12-94)			

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED		
Assistant Examiner		Total Claims      Print Claim for O.G.		
Primary Examiner		DRAWING		
		Sheets Drwg.      Figs.Drwg.      Print Fig.		
PREPARED FOR ISSUE		Application Examiner		
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